

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

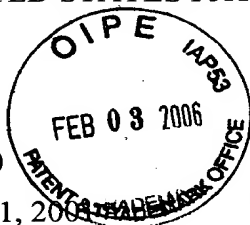
In re application of:

Ekner *et al.*

Appl. No.: 09/788,670

Filed: February 21, 2004

For: **Binary Polynomial Multiplier**



Confirmation No.: 6040

Art Unit: 2193

Examiner: Do, Chat C.

Atty. Docket: 1778.2110000 (0113.00US)

**Second Supplemental Information Disclosure Statement**

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

Sir:

Listed on accompanying Form PTO-1449 are documents that may be considered material to the examination of this application, in compliance with the duty of disclosure requirements of 37 C.F.R. §§ 1.56, 1.97 and 1.98.

Applicants have listed publication dates on the accompanying Form PTO-1449 based on information presently available to the undersigned. However, the listed publication dates should not be construed as an admission that the information was actually published on the date indicated.

Applicants reserve the right to establish the patentability of the claimed invention over any of the information provided herewith, and/or to prove that this information may not be prior art, and/or to prove that this information may not be enabling for the teachings purportedly offered.

This statement should not be construed as a representation that a search has been made, or that information more material to the examination of the present patent application

Ekner *et al.*  
Appl. No. 09/788,670

does not exist. The Examiner is specifically requested not to rely solely on the material submitted herewith.

This Information Disclosure Statement is being filed under 37 C.F.R. § 1.97(b) before the mailing of a first Office Action after the filing of a request for continued examination under 37 C.F.R. § 1.114. No statement or fee is required.

Copies of documents FP1-FP4 and NPL1-NPL25 are provided herewith. However, in accordance with 37 C.F.R. § 1.98(a)(2), no copies of U.S. patents and patent application publications cited on the accompanying Form PTO-1449 are provided.

It is respectfully requested that the Examiner initial and return a copy of the accompanying Form PTO-1449, and indicate in the official file wrapper of this patent application that the documents have been considered.

The U.S. Patent and Trademark Office is hereby authorized to charge any fee deficiency, or credit any overpayment, to our Deposit Account No. 19-0036.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

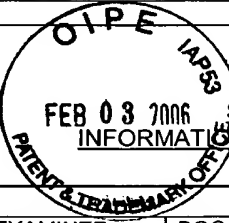


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2/3/06

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 FORM PTO-1449 SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT				ATTY. DOCKET NO. 1778.2110000		APPLICATION NO. 09/788,670	
				FIRST NAMED INVENTOR Hartvig W.J. Ekner			
				FILING DATE February 21, 2001		ART UNIT 2193	
U.S. PATENT DOCUMENTS							
EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	US1	2003/0172254 A1	09/2003	Mandavilli <i>et al.</i>			
	US2	4,491,910	01/1985	Caudel <i>et al.</i>			
	US3	4,511,990	04/1985	Hagiwara <i>et al.</i>			
	US4	4,809,212	02/1989	New <i>et al.</i>			
	US5	4,891,781	01/1990	Omura			
	US6	4,949,250	08/1990	Bhandarkar <i>et al.</i>			
	US7	5,185,713	02/1993	Kobunaya			
	US8	5,517,438	05/1996	Dao-Trong <i>et al.</i>			
	US9	5,537,562	07/1996	Gallup <i>et al.</i>			
	US10	5,669,010	09/1997	Duluk, Jr.			
	US11	5,673,407	09/1997	Poland <i>et al.</i>			
	US12	5,721,892	02/1998	Peleg <i>et al.</i>			
FOREIGN PATENT DOCUMENTS							
EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	FP1	EP 0 681 236 A1	11/1995	EP			N/A
	FP2	EP 0 681 236 B1	11/2000	EP			N/A
OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)							
EXAMINER INITIAL	DOC. REF.	CITATION					
	NPL1	88410 Second Level Cache, Microprocessor Forum, Motorola Inc., November 1991, 20 pages (Bates Numbers L00622-L00641).					
	NPL2	A236 Parallel Digital Signal Processor Chip Programmer's Reference Manual, Oxford Micro Devices, Inc., 1994, 195 pages (Bates Numbers L11184-L11378).					
	NPL3	Bier, J., "DSP16xxx Targets Communications Apps," <i>Microprocessor Report</i> , MicroDesign Resources, September 15, 1997, pages 11-15.					
	NPL4	Diefendorff, K. and Allen, M., "Organization of the Motorola 88110: A Superscalar RISC Microprocessor," Motorola Inc., date unknown, 12 pages (Bates Numbers L00642-00653).					
	NPL5	DSP56000 24-Bit Digital Signal Processor Family Manual, Motorola Inc., 1995, 638 pages (Bates Numbers L08722-L09359).					
EXAMINER					DATE CONSIDERED		
<b>EXAMINER:</b> Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.							

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Page 2 of 5  
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	US13	5,726,927	03/1998	Wolrich <i>et al.</i>			
	US14	5,734,874	03/1998	Van Hook <i>et al.</i>			
	US15	5,740,340	04/1998	Purcell <i>et al.</i>			
	US16	5,752,071	05/1998	Tubbs <i>et al.</i>			
	US17	5,778,241	07/1998	Bindloss <i>et al.</i>			
	US18	5,781,457	07/1998	Cohen <i>et al.</i>			
	US19	5,784,602	07/1998	Glass <i>et al.</i>			
	US20	5,790,827	08/1998	Leung			
	US21	5,793,661	08/1998	Dulong <i>et al.</i>			
	US22	5,822,606	10/1998	Morton			
	US23	5,838,984	11/1998	Nguyen <i>et al.</i>			
	US24	5,864,703	01/1999	Van Hook <i>et al.</i>			

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	FP3	WO 97/07450 A1	02/1997	PCT			N/A
	FP4	WO 97/08608 A1	03/1997	PCT			N/A

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)		
EXAMINER INITIAL	DOC. REF.	CITATION
	NPL6	El-Sharkawy, Mohamed, Ph.D., <i>Digital Signal Processing Applications with Motorola's DSP56002 Processor</i> , Prentice Hall PTR, 1996, pages 43-124 (Bates Numbers L06519-L06601).
	NPL7	Lijun Gao, Sarvesh Shrivastava, Hanbo Lee, Gerald E. Sobelman, "A Compact Fast Variable Key Size Elliptic Curve Cryptosystem Coprocessor," <i>Proceedings of the 7<sup>th</sup> Annual IEEE Symposium on Field-Programmable Custom Computing Machines</i> , April 21-23, 1999, pp. 304-305 (4 pages).
	NPL8	Gwennap, L., "Digital, MIPS Add Multimedia Extensions," <i>Microprocessor Report</i> , MicroDesign Resources, Vol. 10, No. 15, November 18, 1996, pages 1-5.
	NPL9	Gwennap, L., "UltraSparc Adds Multimedia Instructions," <i>Microprocessor Report</i> , MicroDesign Resources, Vol. 8, No. 16, December 5, 1994, pages 1-3.
	NPL10	Hansen, Craig, "Architecture of a Broadband Mediaprocessor," <i>COMPCON96</i> , February 25-29, IEEE, 1996, 8 pages (Bates Numbers L00654-L00661).

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	US25	5,867,682	02/1999	Witt <i>et al.</i>			
	US26	5,880,984	03/1999	Burchfiel <i>et al.</i>			
	US27	5,936,872	08/1999	Fischer <i>et al.</i>			
	US28	5,953,241	09/1999	Hansen <i>et al.</i>			
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EXAMINER INITIAL	DOC. REF.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	FP						Yes No
	FP						Yes No
<b>OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)</b>							
EXAMINER INITIAL	DOC. REF.	CITATION					
	NPL11	Hays, Pat, <i>LX5280 High-Performance RISC-DSP for IP Licensing</i> , at <a href="http://www.lexra.com/presentation/">http://www.lexra.com/presentation/</a> , 27 pages (June 8, 1999).					
	NPL12	<i>i860™ Microprocessor Family Programmer's Reference Manual</i> , Intel Corporation, 1992, 79 pages (Bates Numbers L09361-L09439).					
	NPL13	<i>IBM Technical Disclosure Bulletin</i> , "Pipelined Hardware Multiplier with Extended Precision," Vol. 23, Issue 9, pp. 4322-4323 (February 1, 1981) (5 pages).					
	NPL14	<i>IEEE Standard for Binary Floating-Point Arithmetic</i> , IEEE, 1985, pages i-vi and 1-14.					
	NPL15	Lee, Ruby, "Accelerating Multimedia with Enhanced Microprocessors," <i>IEEE Micro</i> , IEEE, April 1995, pages 22-32 (Bates Numbers L08566-L08576).					
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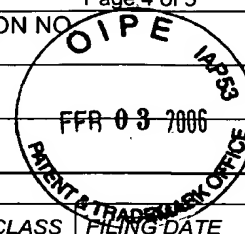
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	US37	6,233,597 B1	05/2001	Tanoue <i>et al.</i>			07/07/1998
	US38	6,295,599 B1	09/2001	Hansen <i>et al.</i>			08/24/1999
	US39	6,349,318 B1	02/2002	Vanstone <i>et al.</i>			10/14/1999
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	FP						Yes No
	FP						Yes No

**OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)**

EXAMINER INITIAL	DOC. REF.	CITATION
	NPL16	Lexra LX5280 Seminar Slides, date unknown, 49 pages.
	NPL17	LX4180, at <a href="http://www.lexra.com/lx4180.html">http://www.lexra.com/lx4180.html</a> , Lexra Inc., 9 pages (Copyright 1998-1999).
	NPL18	Peleg, A. and Weiser, U., "MMX Technology Extension to the Intel Architecture," <i>IEEE Micro</i> , IEEE, August 1996, pages 42-50 (Bates Numbers L07222-L07230).
	NPL19	Piccolo - <i>The ARM Signal Processing Architecture</i> , at <a href="http://www.calab.cs.pusan.ac.kr/TechnicalReport....">http://www.calab.cs.pusan.ac.kr/TechnicalReport....</a> , 12 pages (visited March 6, 2001).
	NPL20	TMS320C1x/C2x/C2xx/C5x Assembly Language Tools User's Guide, Texas Instruments, March 1995, 483 pages (Bates Numbers L07916-L08398).

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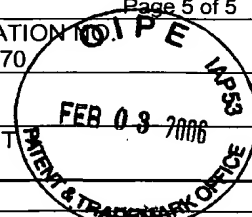
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	FP						Yes No
	FP						Yes No

**OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)**

EXAMINER INITIAL	DOC. REF.	CITATION
	NPL21	<i>TMS320C5x General-Purpose Applications User's Guide</i> , Texas Instruments, July 1997, 167 pages (Bates Numbers L08399-L08565).
	NPL22	<i>TMS32010 User's Guide</i> , Texas Instruments Incorporated, 1983, page 1183.
	NPL23	Turley, Jim and Hakkarainen, Harri, "TI's New 'C6x DSP Screams at 1,600 MIPS," <i>Microprocessor Report</i> , MicroDesign Resources, February 17, 1997, pages 14-17.
	NPL24	<i>VIS™ Instruction Set User's Manual</i> , Sun Microsystems, Inc., 1997, pages i-xii and 1-136.
	NPL25	Yarlagadda, Krishna, "Lexra Adds DSP Extensions," <i>Microprocessor Report</i> , MicroDesign Resources Inc., Vol. 13, Issue 11, August 23, 1999, pages 19-21 (printed from West database, 6 pages).

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